CHANNEL LINK Moving and Shaping Information In Point-To-Point Applications

National Semiconductor
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Tim Novak
Sue Poniatowski
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This application note explains National Semiconductor's CHANNEL LINK chipset and discusses related issues in point-to-point subsystem communications. A background on CHANNEL LINK will be offered followed by several high-speed point-to-point applications that build on the basic serial link transmission topology. System issues such as various bus widths, error detection and control line timing are discussed. The concept of a virtual backplane transceiver is also introduced. Finally, design considerations for high-speed serialized links are presented.

WHAT IS CHANNEL LINK?

CHANNEL LINK is a chipset of interface devices configured to support high-speed point-to-point data transmission between two backplanes, card cages and/or equipment cabinets which are physically separated by distances of up to 10 meters. Each CHANNEL LINK chipset consists of one transmitter and one receiver. The CHANNEL LINK transmitter converts parallel TTL/CMOS data into multiplexed LVDS (Low Voltage Differential Signaling) serialized data streams for transmission over an economical medium such as twisted pair copper wire. The CHANNEL LINK receiver converts the LVDS data streams back into parallel TTL/CMOS data. LVDS is a differential signaling technology designed to support applications requiring high speed data transfer, common mode noise rejection, and low power consumption.

WHY IS CHANNEL LINK NEEDED?

This chipset is an ideal means to solve speed, cable size, power and EMI problems typically found in extended pointto-point applications. These applications are common in the telecommunications equipment industry. The emergence of new broadband transmission equipment for fiber- and coax-based multimedia systems and next generation cellular infrastructure base stations requires that backplane speeds increase to rates much faster than seen in past architectures. CHANNEL LINK has applications in equipment such as Host Digital Terminals, Optical Network Units, Fiber Nodes, Broadband Switches, Tandem Switches, Digital Cross-Connects and Cellular Basestations.

ADVANTAGES OF USING CHANNEL LINK

- Current CHANNEL LINK chipsets allow interface to backplane busses running at speeds of 20 MHz to 40 MHz thus providing an overall throughput up to 1.12 Gbps (140 Mbytes/sec).
- The multiplexing of parallel TTL/CMOS data allows the data to travel over a narrow bus width between the two equipment racks. The ability to utilize fewer and more economical interconnect wires results in a cost savings. The 21-bit CHANNEL LINK chipset requires four wire pairs (3 pairs for data and one pair for clock) between transmitter and receiver. The 28-bit CHANNEL LINK chipset requires five wire pairs (4 pairs for data and one pair for clock). In comparison to a standard parallel approach, a near 80% reduction in cable width is attained and the probability of transmission errors due to cable skew is reduced.

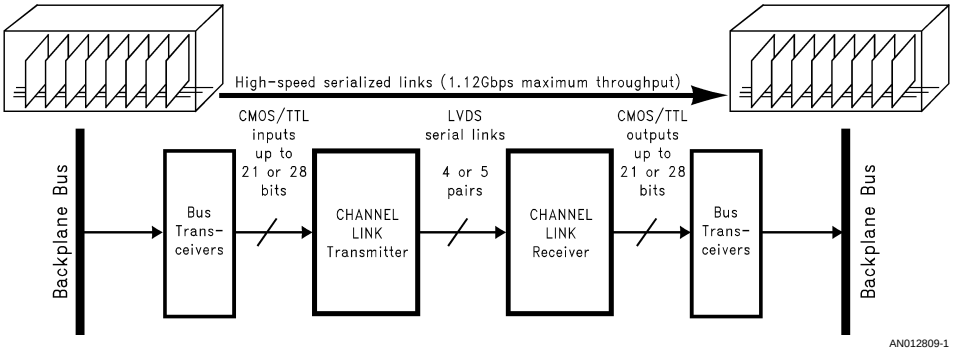

FIGURE 1. CHANNEL LINK Subsystem Communications Solution

- CHANNEL LINK is a low power means of transporting high-speed data over an interconnect. LVDS technology represents a significant decrease in power to comparable high-speed transmission devices such as PECL. The CHANNEL LINK transmitter has a dynamic loaded Icc of 35 mA (typical) while the CHANNEL LINK receiver is 60 mA (typical). CHANNEL LINK also includes a Power-down mode which reduces total device power to < 5 µW (typical).

- CHANNEL LINK utilizes LVDS technology on the high-speed serialized links. LVDS has a signal swing of 300 mV and is centered at +1.20V. The 300 mV differential signals of LVDS provide the advantage of reducing noise impact such as crosstalk and EMI when transmitting very high data rates over wire. LVDS has demonstrated lower spectral content (EMI) than competing technologies such as RS-422, PECL and TTL. Low EMI translates to less noise on a cable in point-to-point transmission applications. In addition, LVDS supports an input voltage range of Ground to +2.4V. The input voltage range allows for a ±1.0V shifting of the signal center (+1.2V) due to ground potential differences and noise. This provides a reliable margin against ground shifting that might occur between transmitter and receiver on the serialized links.
- Both ends of the CHANNEL LINK chipset utilize an on-chip PLL that requires no extemal components. The PLL ensures accurate phase alignment at the transmit and receive outputs.

NATIONAL'S CHANNEL LINK OFFERING

The 21-bit chipset is part number DS90CR211/212 (possible user configuration: two payload bytes + two parity bits + 3 control bits). The 28-bit chipset is part number DS90CR281/282 (possible user configuration: three payload bytes + three parity bits + one control bit). The backplane bus clock for each must operate between the frequency range of 20 MHz to 40 MHz and both ends of the chipset must be powered from a +5V power source. Future chipset derivatives will address additional throughput, power and other bottleneck issues.

APPLICATIONS FOR CHANNEL LINK

The 21-bit and 28-bit wide CHANNEL LINK devices provide application flexibility for different bus extensions. Additionally, the chipset devices can be configured in a parallel fashion. Parallel configurations can result in CHANNEL LINK supporting numerous implementations of combined data, address, parity and control signals. Three such configurations using the 21-bit 90CR211/212 chipset are offered as examples.

Note that the examples shown in the next several figures implement BTL transceivers at the backplane bus parallel interface. National's BTL transceivers are commonly used in many systems where the backplane bus is heavily loaded and runs at speeds in excess of 20 MHz. National also offers a complete line of ABT transceivers for those applications where the combined effects of loading and/or speed are less stringent. The designer should note that BTL and ABT transceivers may require additional control logic to arbitrate the backplane bus, and backplane clock synchronization may be required in some applications. These topics are beyond the scope of this application note, as they are application specific.

16-BIT BUS EXTENSION

In a 16-bit bus application (see *Figure 2*), TTL-level data and clock coming from BTL transceivers which interface the backplane bus arrive at the "TxIN" parallel inputs of the CHANNEL LINK transmitter. The clock associated with the bus is also connected to CHANNEL LINK at the dedicated "TxCLKIN" input. The on-chip PLL synchronizes this clock with the parallel data at the input. The parallel data is then multiplexed/mapped into three differential line drivers which perform the TTL to LVDS conversion. The transmit clock is also converted to LVDS and presented to a separate line driver. The synchronized LVDS data and clock traverse the cable to the CHANNEL LINK receiver. The CHANNEL LINK receiver recovers the LVDS data and clock and performs a conversion back to TTL. Data is then unmapped/demultiplexed into a parallel format. An on-chip PLL synchronizes the received clock with the parallel data and then all are presented at the parallel output port of the receiver.

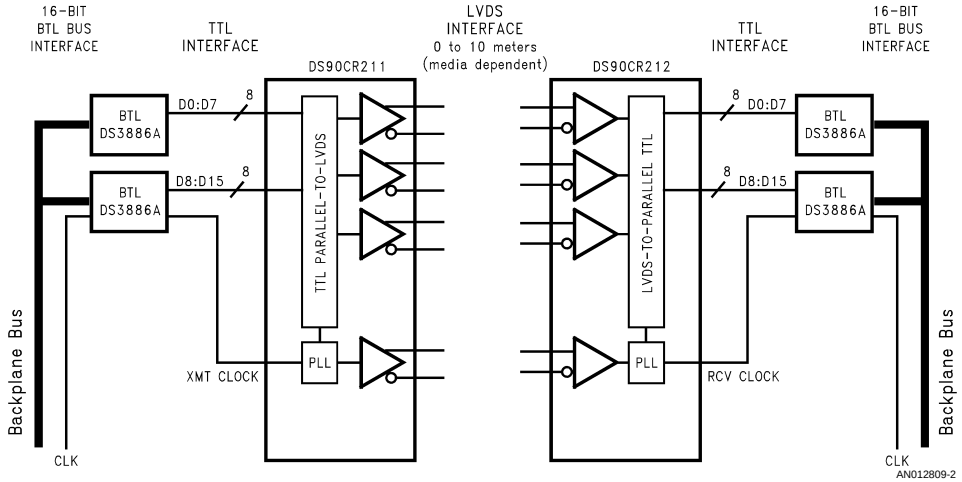

FIGURE 2. CHANNEL LINK 16-Bit Bus Extension

16-BIT BUS EXTENSION WITH PARITY

Figure 3 builds on the previous example by adding a parity feature on both ends of the link. The addition of parity generation/checking provides assurance that the data reliably crosses the link. National's 74ABT899 is a low-cost parity generator. Each transmit-side ABT899 takes the TTL data from the corresponding BTL transceiver, performs a parity calculation over the byte and then transparently passes each

byte with its calculated parity value on to the parallel input of the CHANNEL LINK transmitter. The clock associated with the data bus is directly connected to the dedicated clock input on CHANNEL LINK. The on-chip PLL synchronizes this transmit clock with the eighteen parallel bits (16 data + 2 parity) at the input. The synchronized LVDS data/parity and clock traverse the cable to the CHANNEL LINK receiver.

The CHANNEL LINK receiver recovers the LVDS data/parity and clock and performs a conversion back to TTL. Each receive-side ABT899 is configured to perform a parity calculation over its corresponding input byte and compares this calculated parity with the value of the received parity bit. The ABT899 will assert its Parity Error output if a mismatch is detected. The Parity Error outputs are logically OR'd in this example.

PARITY COMPLEMENTS CHANNEL LINK

Errors rarely occur in most transmission systems. In fact, bit-errors < 1 in 10^{12} bits are achievable. Parity alone provides an extra degree of reliability by detecting single-bit errors. Multiple-bit errors can be detected too when the parity method is combined with CHANNEL LINK'S serial bit mapping locations. The designer has the flexibility of interleaving the parallel data into any one of the three serial streams by breaking up the byte + parity data coming out of each ABT899 and selecting any input configuration at the parallel input of the CHANNEL LINK transmitter. Care must be taken to ensure that the configuration is emulated at the CHANNEL LINK receiver outputs so that the original byte + parity data is reconstructed and input to its corresponding ABT899 at the receiving end. The bit map locations of the serialized links are shown in *Figure 4* and *Figure 5* for the DS90CR211/212 and DS90CR281/282, respectively.

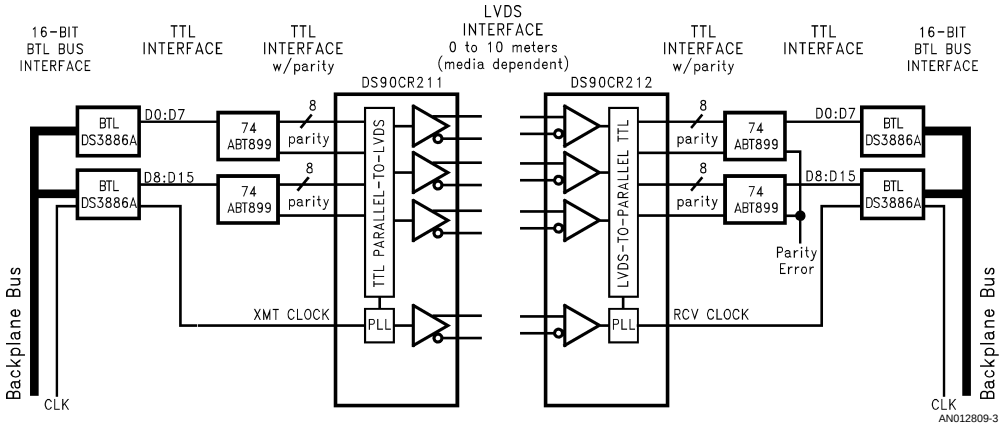

FIGURE 3. CHANNEL LINK 16-Bit Bus Extension With Parity Check

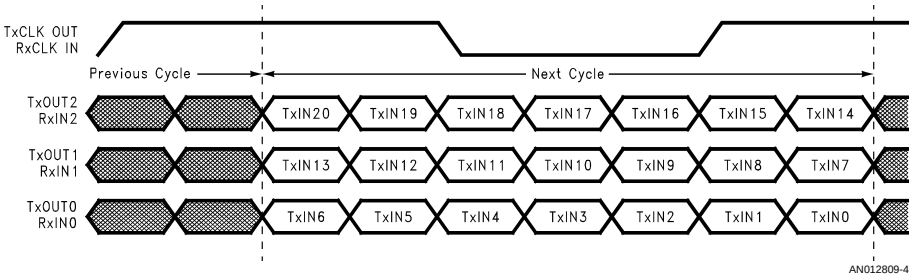

FIGURE 4. Bit Map Locations of Serialized Links (DS90CR211/212)

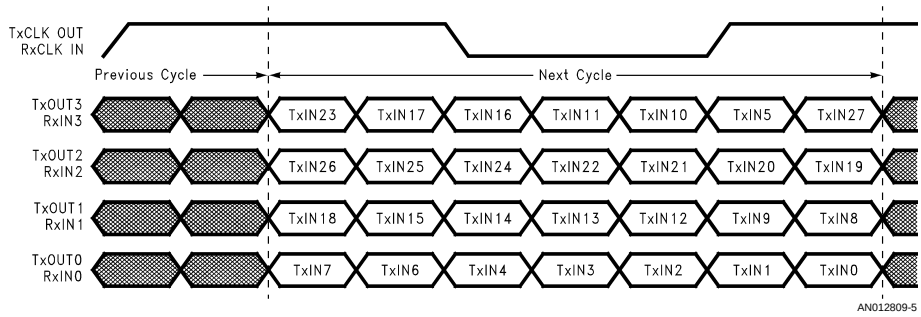

FIGURE 5. Bit Map Locations of Serialized Links (DS90CR281/282)

32-BIT BUS EXTENSION WITH PARITY AND DELAY LINES

Figure 6 builds on the previous example by adding delay lines at the receiving end of the link. It also depicts a 32-bit bus which is quite common in many telecom subsystem architectures. The addition of delay lines on “Side-Z” of the interface allows the user to closely emulate the phase relationships/timing characteristics of control signals (e.g. R/W, ALE, DS) seen on “Side-A” over on to “Side-Z”.

The example in *Figure 6* assumes that the backplane bus and clock are synchronous while control signals will typically occur *n*-nanoseconds (application specific) after the clock/bus transitions.

This allows the bus to setup and stabilize before control signals are asserted. It is important to note that all parallel input bits to the CHANNEL LINK transmitter must meet a minimum setup time before the next rising clock edge. It is this rising clock edge which latches in all the parallel input signals. A timing diagram in *Figure 7* shows an example of how the bus, clock and control signals all interact. It also shows the effect of the delayed control signals at the output on “Side- Z” of the interface. The value of each delay line should be selected according to the timing difference between data/clock and each individual control signal as seen on “Side-A”.

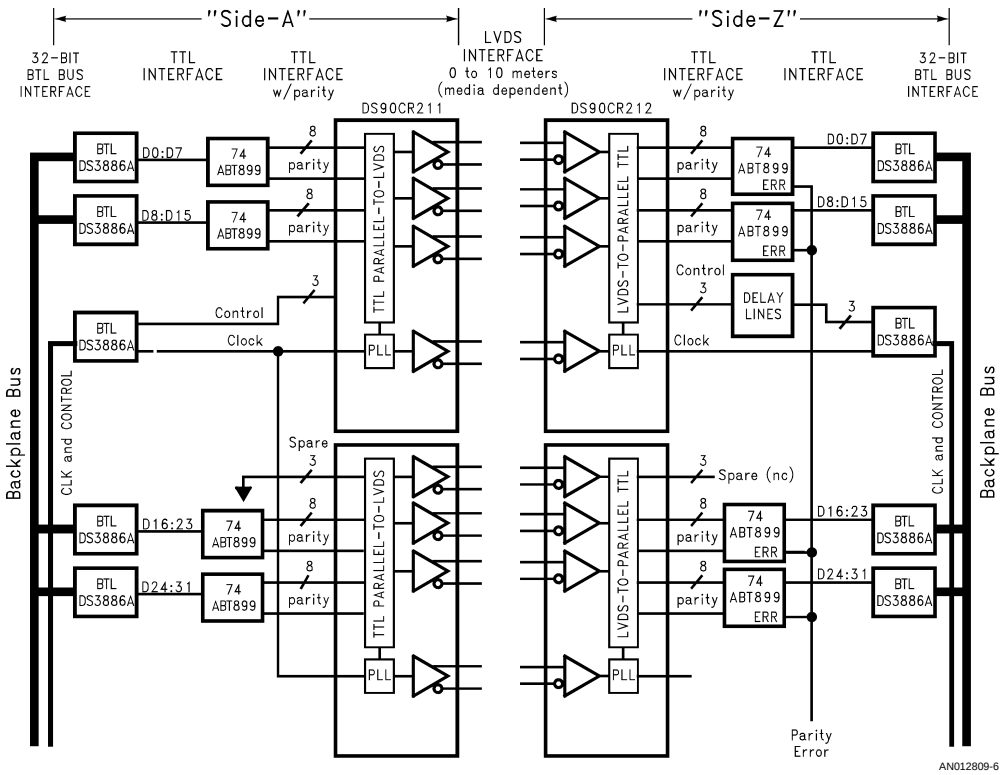

FIGURE 6. CHANNEL LINK 32-Bit Bus Extension With Parity Check and Control Signals

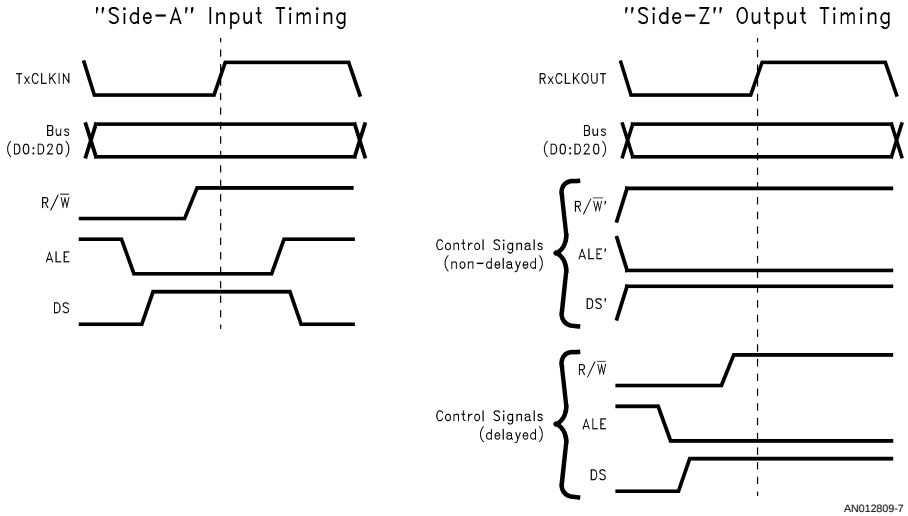

FIGURE 7. Clock, Bus and Control Signal Timing Diagrams

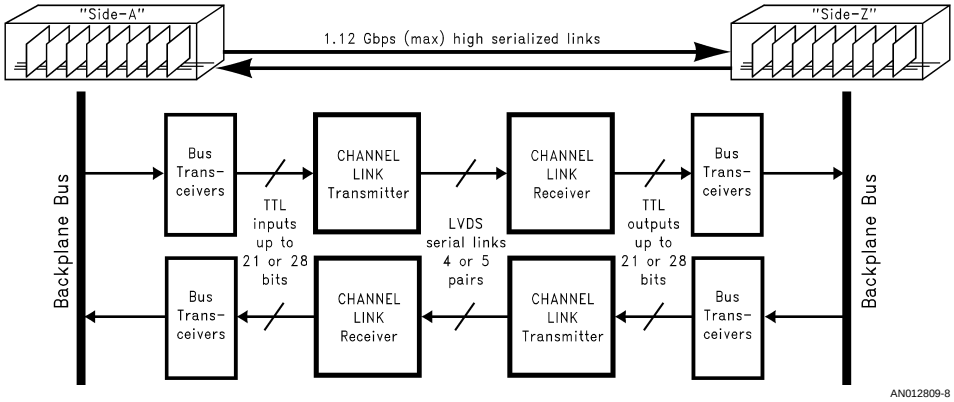

FIGURE 8. Using CHANNEL LINK in a Virtual Backplane Transceiver Application

LOW-COST VIRTUAL BACKPLANE TRANSCEIVER

Figure 8 presents CHANNEL LINK in an application as a Virtual Backplane Transceiver (VBT). The concept of a VBT can be achieved by implementing individual CHANNEL LINK chipsets in both directions of subsystem serialized links.

Depending on the application, the designer will face varying choices when implementing a VBT. In addition to the devices shown in *Figure 8* above, functions such as parity and delay lines for control signals could be included. Using additional circuitry, half-duplex or full-duplex operation can be achieved by configuring the clock and control lines properly.

The designer may choose to implement a clock oscillator at each end of the link which is independent of the backplane bus clock and then use a PLL to synchronize CHANNEL LINK's parallel I/O to the backplane bus. Re-synchronizing FIFOs may also be required.

CONCLUSION

This application note demonstrates that the CHANNEL LINK chipset architecture in conjunction with LVDS technology provides the high bandwidth interface necessary for leading edge point-to-point subsystem communications that are common in today's telecommunications infrastructures. The conversion from parallel TTL to serial LVDS allows for a narrow interface link. A narrower interface means lower cable costs. The high speed of the LVDS techhology supports the high data transfer rates required. EMI problems typically associated with such high speed transmissions are addressed by the low signal swing and differential nature of LVDS. LVDS with its high speed capabilities, will allow future products in the CHANNEL LINK chipset to support the ever increasing needs for bandwidth. National's CHANNEL LINK provides the solution for high-speed subsystem communications!

DESIGN CONSIDERATIONS OF CHANNEL LINK

This section is intended to present a short summary of considerations which the designer should implement in order to obtain maximum performance from CHANNEL LINK. A more thorough explanation of helpful design hints can be found in all of the following National Semiconductor Application Notes:

1. "PCB Design Guidelines for LVDS Technology" AN-1035
2. "EMI/RFI Board Design" AN-643
3. "Data Transmission Lines and Their Characteristics" AN-806
4. "Transmission Line RAPIDESIGNER© Operation and Applications Guide" AN-905
5. "A Practical Guide to Cable Selection" AN-916

CABLES

A cable interface between the transmitter and receiver needs to support the differential LVDS pairs. The 21-bit CHANNEL LINK chipset (DS90CR211/212) requires four pairs of signal wires and the 28-bit CHANNEL LINK chipset (DS90CR281/282) requires five pairs of signal wires. The ideal cable/connector interface would have a constant 100Ω differential impedance throughout the path. It is also recommended that cable skew remain below 350 ps (@ 40 MHz clock rate) to maintain a sufficient data sampling window at the receiver.

In addition to the four or five cable pairs that carry data and clock, it is recommended to provide at least one additional conductor (or pair) which connects ground between the transmitter and receiver. This low impedance ground provides a common mode return path for the two devices. Some of the more commonly used cable types for point-to-point applications include flat ribbon, flex, twisted pair and Twin-Coax. All are available in a variety of configurations and options. Flat ribbon cable, flex and twisted pair generally perform well in short point-to-point applications while Twin-Coax is good for short and long applications. When using ribbon cable, it is recommended to place a ground line between each differential pair to act as a barrier to noise coupling between adjacent pairs. For Twin-Coax cable applications, it is recommended to utilize a shield on each cable pair. All extended point-to-point applications should also employ an overall shield surrounding all cable pairs regardless of the cable type. This overall shield results in improved transmission parameters such as faster attainable speeds, longer distances between transmitter and receiver and reduced problems associated with EMS or EMI. The high-speed transport of LVDS signals has been demonstrated on several types of cables with excellent results. However, the best overall performance has been seen when using Twin-Coax cable. Twin-Coax has very low cable skew and EMI due to its construction and double shielding. All of the design considerations discussed here and listed in the supplemental appli-

cation notes provide the subsystem communications designer with many useful guidelines. It is recommended that the designer assess the tradeoffs of each application thoroughly to arrive at a reliable and economical cable solution.

BOARD LAYOUT

To obtain the maximum benefit from the noise and EMI reductions of LVDS, attention should be paid to the layout of differential lines. Lines of a differential pair should always be adjacent to eliminate noise interference from other signals and take full advantage of the noise canceling of the differential signals. The board designer should also try to maintain equal length on signal traces for a given differential pair. As with any high speed design, the impedance discontinuities should be limited (reduce the numbers of vias and no 90 degree angles on traces). Any discontinuities which do occur on one signal line should be mirrored in the other line of the differential pair. Care should be taken to ensure that the differential trace impedance match the differential impedance of the selected physical media (this impedance should also match the value of the termination resistor that is connected across the differential pair at the receiver's input). Finally, the location of the CHANNEL LINK TxOUT/RxIN pins should be as close as possible to the board edge so as to eliminate excessive pcb runs. All of these considerations will limit reflections and crosstalk which adversely effect high frequency performance and EMI.

UNUSED INPUTS

All unused inputs at the TxIN inputs of the transmitter must be tied to ground. All unused outputs at the RxOUT outputs of the receiver must then be left floating.

TERMINATION

Use of current mode drivers requires a terminating resistor across the receiver inputs. The CHANNEL LINK chipset will normally require a single 100Ω resistor between the true and complement lines on each differential pair of the receiver input. The actual value of the termination resistor should be selected to match the differential mode characteristic impedance (90Ω to 120Ω typical of the cable media). *Figure 9* shows an example. No additional pull-up or pull-down resistors are necessary as with some other differential technologies such as PECL. Surface mount resistors are recommended to avoid the additional inductance that accompanies leaded resistors. These resistors should be placed as close as possible to the receiver input pins to reduce stubs and effectively terminate the differential lines.

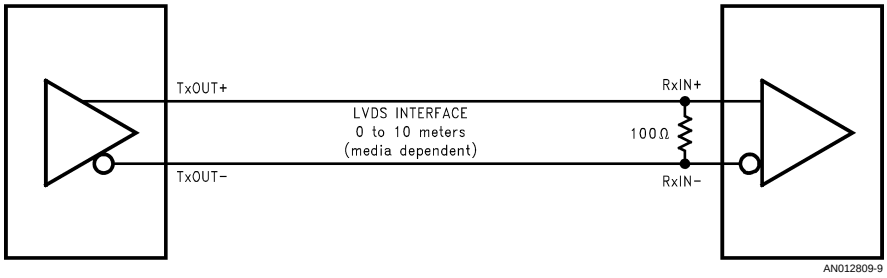

FIGURE 9. LVDS Serialized Link Termination

DECOUPLING CAPACITORS

Bypassing capacitors are needed to reduce the impact of switching noise which could limit performance. For a conservative approach three parallel-connected decoupling capacitors (Multi-Layered Ceramic type in surface mount form factor) between each V_{CC} and the ground plane(s) are recommended. The three capacitor values are 0.1 µF, 0.01 µFand 0.001 µF. An example is shown in *Figure 10*. The designer should employ wide traces for power and ground and ensure each capacitor has its own via to the ground plane. If board space is limiting the number of bypass capacitors, the PLL V_{CC} should receive the most filtering/bypassing. Next would be the LVDS V_{CC}pins and finally the logic V_{CC} pins.

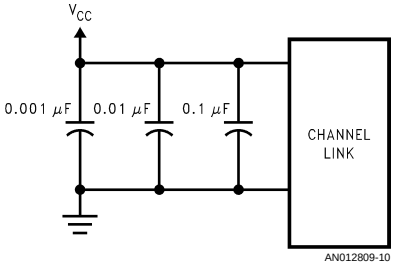

FIGURE 10. CHANNEL LINK Decoupling Configuration

CLOCK JITTER

The CHANNEL LINK devices employ a PLL to generate and recover the clock transmitted across the LVDS interface. The width of each bit in the serialized LVDS data stream is one-seventh the clock period. For example, a 40 MHz clock has a period of 25 ns which results in a data bit width of 3.57 ns. Differential skew (Δt within one differential pair), interconnect skew (Δt of one differential pair to another) and clock jitter will all reduce the available window for sampling the LVDS serial data streams. Care must be taken to ensure that the clock input to the transmitter be a clean low noise signal. Individual bypassing of each V_{CC} to ground will minimize the noise passed on to the PLL, thus creating a low jitter LVDS clock. These measures provide more margin for channel-to-channel skew and interconnect skew as a part of the overall jitter/skew budget.

COMMON MODE vs DIFFERENTIAL MODE NOISE MARGIN

The typical signal swing for LVDS is 300 mV centered at +1.2V. The CHANNEL LINK receiver supports a 100 mV threshold therefore providing approximately 200 mV of differential noise margin. Common mode protection is of more importance to the system's operation due to the differential data transmission. LVDS supports an input voltage range of Ground to +2.4V. This allows for a ±1.0V shifting of the center point due to ground potential differences and common mode noise.

POWER SEQUENCING AND POWERDOWN MODE

Outputs of the CHANNEL LINK Transmitter remain in TRI-STATE® until the power supply reaches 3V. Clock and data outputs will begin to toggle 10 ms after V_{CC} has reached 4.5V and the Powerdown pin is above 2V. Either device may be placed into a powerdown mode at any time by asserting the Powerdown pin (active low). Total power dissipation for each device will decrease to 5 µW (typical).

The CHANNEL LINK chipset is designed to protect itself from accidental loss of power to either the transmitter or receiver. If power to the transmit board is lost, the receiver clocks (input and output) stop. The data outputs (RxOUT) retain the states they were in when the clocks stopped. When the receiver board loses power, the receiver inputs are shorted to V_{CC} through an internal diode. Current is limited (5 mA per input) by the fixed current mode drivers, thus avoiding the potential for latchup when powering the device.

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National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
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National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179